Brushless Motor Power Control - Without Power

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Abstract - In hundreds of millions of computers, a shutdown sequence lasting several seconds carefully manages the delicate HDD mechanics - without a power supply. With so much riding on powerless operation, power down issues often dominate the design of the Power LSI chips. In this article, the art and science of designing Power LSI to manage an orderly HDD shutdown is discussed. Power chip and systems issues are introduced, with a brief outline of previous approaches. The enhanced Western Digital LSI solution is then presented, with a theory of operation, a working discussion and a description of power control features required to support final operations.

Additionally, head wear due to the roughened parking surface can occur as the platters spin down. So the spindle motor must be stopped as quickly as possible once the head is parked.

II Power Down Park and Brake - The Old Way

In previous power driver chip designs, the 12 volt supply diode isolation (D1 in figure 1) allowed the back EMF from the motors to be used as a generator to provide a lossy, nominal supply voltage when power is lost. The AC motor back EMF voltage waveforms drive current through the natural parasitics built into the power chip output stages, which is rectified and filtered on C1. In figure 1a, the interaction of the AC waveforms of the 3 phase motor with the output FET drivers is illustrated. At the instant shown, phase A is providing positive voltage, while phase B is negative. This causes current to be sourced from ground through D6, through phase B and A, and out D3 into C1. From there, current is supplied to the head park circuitry, which drives the voice coil motor (VCM) that moves the heads. (The equivalent VCM driver circuit is shown in figure 1b.)

I. Why We Need Power Down Management

Disk Drives today use recording heads with fly heights so low that surface effects weld the head onto the media unless the media is spinning, causing damage to the head and media. The predominant industry solution is to provide a specially roughened landing area (the park zone) at the inner diameter of the media where the head can land. Moving the heads to this zone is called parking the heads. Since at low media RPM the air bearing supporting the heads is not stiff, parking must be done at a low and controlled velocity.
Figure 1a – “Old Way” - Natural Parasitics Provide DC Power During Shutdown

“Old Way” Equivalent Circuit (1b)
This arrangement provides livable, unregulated voltage during power down, from which a simple constant voltage is supplied to park the heads. An RC timer ends the head parking period and the spindle motor driver FETs are then shorted. This causes the spindle motor to brake and stop the media in a minimum of time and limiting head wear. This approach, while in general use, has several limitations:

**Limited Power Capability.** The circuit model (figure 1b) has 2 lossy substrate diodes in series with about 2 to 3 times the average motor winding resistance. Since the chip requires about 6 volts to operate, available current for the VCM system is very limited. Depending on the final RPM design of the product, usually less than 100 mA is available for the head parking.

**Mechanical Factors.** Head latch bounce occurs before park is complete, reversing the VCM back EMF and raising required currents right when the spindle motor back EMF voltage that supplies power has decayed to its lowest point. These high peak currents could shut down the chip and leave the head on the media if the mechanics are not well characterized. The spindle motors had to be designed to give the optimum available voltage and current for parking, which put fairly strict limits on the operating RPM range of the product.

**High Peak Currents.** The power required to stop the media is all dumped through the output DMOS FET stages. Since there is no way to keep additional circuits alive after the FETs short, the FETs must stay on once they are activated. These FETs must handle worst case current from the motor in a dead short, which puts strict lower limits on the impedance of the motor winding.

Careful chip design and manufacturing process procedures had to be developed to ensure that parasitics which are normally reverse biased would not drain the FET gates and halt the braking action.

**Power Down Transition and Parasitic Management.** By far the most difficult problem to manage was the chip power handling configuration during power down. The power chip has, in addition to 12V and 5V external supplies, internal regulators that handle various power down circuitry. A charge pump develops 20 to 30 volts for biasing the top side FETs. A smooth transfer between the external and internal supplies had to be made. Additionally, at large currents, output stage structures suddenly no longer look like FETs. Isolation structures become parasitic transistors that drain internal nodes through various sneak paths on the chip, disrupting circuitry and rendering power down operation questionable. Finally, logic and analog circuitry had to be glitch free during the uncertain power down period, necessitating careful partitioning.

It was found that these transition issues demanded the simplest possible shutdown circuitry, and dictated not only design, but also silicon debug and process issues. As new LSI has required additional 3.3 volt monitoring and sequencing, and power down management for the other devices in the hard drive, power sequencing was quickly becoming unmanageable. A new approach was needed.

**III New Approach: Design Objectives**

The revised power down management scheme was set up to gain control of the variables that influenced or limited the design, even where more complexity was demanded to do so. This approach would provide flexibility and, paradoxically, shorter design cycles. The
result was the **Boost Brake Power Down Management System (BBS)**.

### IV Boost Brake System (BBS)

The power down system shown in figure 2 was introduced with the current generation Power LSI chip, the Orca. A fundamental improvement is the use of the motor winding inductance as a boost inductor, producing a higher (but still unregulated) voltage on the isolated power supply node (figure 3). With additional voltage available, and with the power supply environment now controlled exclusively by the Power LSI chip, it becomes possible to handle power control, thermal control, power routing, current limiting, and other features, allowing a sophisticated extension of the chip’s power handling capabilities and shutdown management while reducing exposure to the transition, parasitic and bias issues.

The BBS design (refer to figure 2) has these important elements:

1. A simple **fixed duty cycle motor winding short**, created by overriding the normal commutation sequence and routing the PWM Generator to short all 3 bottom FETs (Q2, Q5 and Q8). Motor inductive flyback then crudely boosts the back EMF voltage presented to the Vpwr node through the parasitic diodes. Depending on duty cycle, the voltage can be boosted by a factor of 3 or more.

2. A power **filter capacitor** (C1) maintains voltage during the initial power loss period while winding current builds up, and filters the shorted winding voltage waveform.

3. A **current limit circuit** (Q3, Q6, Q9) shortens the duty cycle if peak currents get too high for the chip to handle. This feature, made possible by the higher chip voltage, allows the chip to operate at its own maximum possible current regardless of winding impedance. Since motor winding impedance goes down quickly as design RPM goes up, the chip is capable of driving a much wider RPM range and higher loads.

4. An **overvoltage clamp** (D2) provides overvoltage protection against the crude boost circuit. If the Vpwr voltage is boosted until this diode turns on, motor energy will then dump into this rugged external zener diode instead of being dissipated in the motor windings or the power chip.

5. If it is desired to conserve spin speed, the boost action can optionally be prolonged using the **Overvoltage Comparator**, which shuts down the boost below the clamp diode voltage. Since no current is dumped into the clamp, the drive will then spin down at a much slower rate, dissipating energy only as windage losses in the motor and media. By using the comparator and setting the clamp voltage, the designer now has several **thermal management** options; park timing can be extended to several seconds for a high RPM drive, energy can be dissipated in the diode clamp, or it can be absorbed directly in the chip.

6. A **BBS STOP timer** optionally watches the length of time that current limit is in operation. If no current limit occurs for approximately two motor cycles, then the final brake can commence without generating excessive currents in the FETs.

7. Sophisticated **head park** and latch control circuitry (not shown) is now possible, since adequate voltage and current is available and power transfer is managed by the chip. Various park schemes have been added to accommodate a variety of mechanical configurations.
Figure 2 Boost Brake Block Diagram
V Circuit Operation

The simple circuitry shown produces a complex and sophisticated power down sequence. Basic circuit waveforms are shown in figure 3.

Region I: Motor Current Buildup

At the beginning of the waveforms, loss of power is detected. The Orca chip immediately sends a power on reset signal to halt the rest of the drive system, and starts the power down sequence. A fixed duty cycle short is applied to all three spindle windings to build up current in the motor; inductive flyback causes this current to find its way back to the supply through the parasitic diodes on the DMOS FETs, to provide power as quickly as possible to the Vpwr node. Since current builds in the motor, braking action also begins and the RPM starts dropping.

Power needs are critical in region I because during this period the Orca stops the head motion and begins the park sequence. Sudden, large VCM coil currents are needed to quickly decelerate the heads, as power can be lost in the middle of a seek operation. Capacitor C1 makes up the difference between what the spindle motor provides and the VCM demand current.

Region II: Current Limit

As current builds up in the windings, current limit begins to reduce the shorting duty cycle, initiating region II. The voltage on the Vpwr node stops falling due to the reduced duty cycle and higher current.

Region III: Voltage Rise

As the duty cycle drops back, more current recirculates to the Vpwr node, so the Vpwr node voltage begins to rise. Depending on the motor windings, region II and III may overlap.

Region IV: Voltage Clamped Deceleration

In region IV, voltage is clamped by the power zener diode (Path A in Figure 3). Since motor current is high, the zener begins dissipating several watts of power.
This ability to put power dissipation outside of the chip is one reason the chip can be put in a smaller package even though it can handle much higher RPM.

Typically, final head parking occurs in this region. Instead of the 100 milliamps previously available, this approach can provide up to an amp of peak current to the VCM, a 10:1 improvement. The higher current removes the worry of head bounces and peak loading.

More importantly, instead of a constantly sagging voltage at Vpwr, the Power LSI chip now has comfortable headroom. This greatly simplifies internal circuit design and relieves circuit designers of another dimension of problems, namely power transfer glitches during this period.

Additionally, the Vpwr internal node removes the effects of arbitrary sequencing by the computer power supply. The circuit designer now has control of his own destiny, and can plan internal circuitry accordingly, instead of worrying about power transfer with a myriad of external power up/power down conditions.

Path B shows the second option, which is to use the overvoltage option to limit the voltage. Using this option reduces the current in the motor dramatically, reducing the loss of spindle motor RPM and allowing more time to execute head parking or other shutdown algorithms.

As the motor RPM drops, the spindle drops periodically out of current limit. Eventually, one or two spindle commutation cycles goes by without any current limit occurring at all. When this happens, full brake can be applied. The Orca chip may wait an additional period of time, however, if longer park timing is needed, using the second timer.

Note that in all cases, although motor currents can be quite high, they are limited and controlled to a safe level that the chip can handle without parasitic effects. Chip current and peak power are thus now in the hands of the circuit designer.

Region V: Final Brake

After all the spindown requirements have been met and the head is parked, it is time to do the final brake. The FETs are shorted completely, motor current jumps slightly, and the motor decelerates to a stop as quickly as possible. The current limit is briefly kept alive until Vpwr sags to an unsupportable voltage. If current limit is again detected while the current detection circuitry has voltage support, the limited duty cycle can be resumed again.

VI What Were The Results?

The following table gives an idea of the improvement in power down performance, and indirectly in general chip performance, that the boost brake system provided for a typical high RPM application.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Previous Value</th>
<th>Orca Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Park Timing</td>
<td>0.38 seconds</td>
<td>1.5 seconds</td>
<td>4:1 improvement</td>
</tr>
<tr>
<td>Park Operation</td>
<td>Voltage</td>
<td>Active Decel</td>
<td>Sophisticated Park Algorithms Added</td>
</tr>
<tr>
<td>Peak Park Current</td>
<td>100 mA</td>
<td>1 Amp</td>
<td>10:1 improvement</td>
</tr>
<tr>
<td>-------------------</td>
<td>--------</td>
<td>-------</td>
<td>-----------------</td>
</tr>
<tr>
<td>Park RPM</td>
<td>90%</td>
<td>50%</td>
<td>Depends on motor</td>
</tr>
<tr>
<td>% of design speed</td>
<td></td>
<td></td>
<td>Reduces Head Wear</td>
</tr>
<tr>
<td>Chip RPM Range</td>
<td>4500/5400</td>
<td>4500/10,000</td>
<td>Load Current = RPM (^{2.5})</td>
</tr>
</tbody>
</table>

Perhaps the most important advancement, though, was in development time. In the HDD marketplace, where time to market is king, a Power LSI chip takes three times as long as a full custom digital chip to develop, making it one of the longest lead items in the drive to develop. Parasitic issues and leakage problems frequently require complete reprocessing and major redesign to correct. By taking on the additional load of providing power and load control and putting supply transients under control of the circuit designers, time to working silicon was dramatically reduced. This provided schedule relief and actually reduced design risk. Another less obvious risk reduction was also realized; long projects invite change. Additional midstream feature changes could be avoided by shortening the design cycle.

An additional benefit was smooth systems integration. Since most of the variables are now controlled, there is little doubt the power down management system will work as intended. This allows faster HDD program development.

Should you turn off your computer’s power at night? The optimum decision will depend on ever changing head/media technology, bearing life and other design factors. But rest assured; when you do turn off the power, sophisticated power management will confidently, dependably and safely shut down your drive.